

Memory Signal Integrity Report

- ❖ Foxconn_SKT
- ❖ K18X001.00
- ❖ H5AN8G6NDJR-VKC

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- Released Date : **2021-09-13**

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System History

Release Date	Contents	Remarks
2021-01-28	H5AN8G6NCJR-VKC	U2
2021-02-01	H5AN4G6NBJR-VKC	U5
2021-03-12	H5AN8G6NCJR-VKC	U2
2021-09-13	H5AN8G6NDJR-VKC	U2

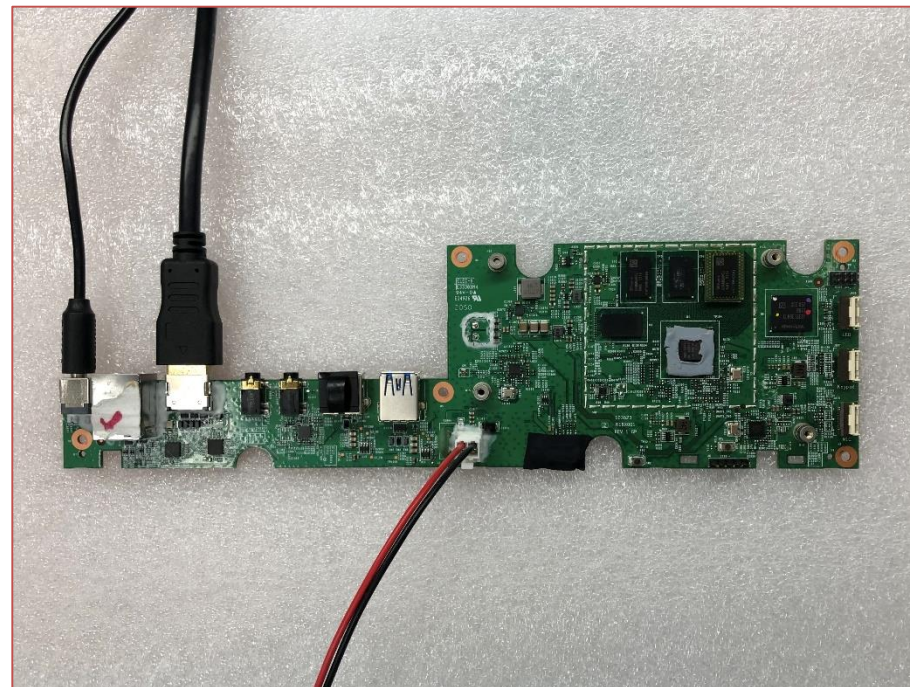
■ System & Memory Information

Model Name	K18X001.00
Application type	OTT STB
PCB Number and Revision	V115
Chipset	Synaptics VS-550
BIOS Version & Date	-
DRAM Part Number	H5AN8G6NDJR-VKC
DRAM Operating Frequency	1333MHz (DDR4-2666)
DRAM Density	8Gb
DRAM pieces	2ea
DRAM Width	x16

■ Equipment & Test Condition

Oscilloscope	KEYSIGHT DSA91304A
Probes	1169B
Temperature	25°C
VDD / Vref-CA	1.200V / 0.600V

■ System picture



Judgment & Summary

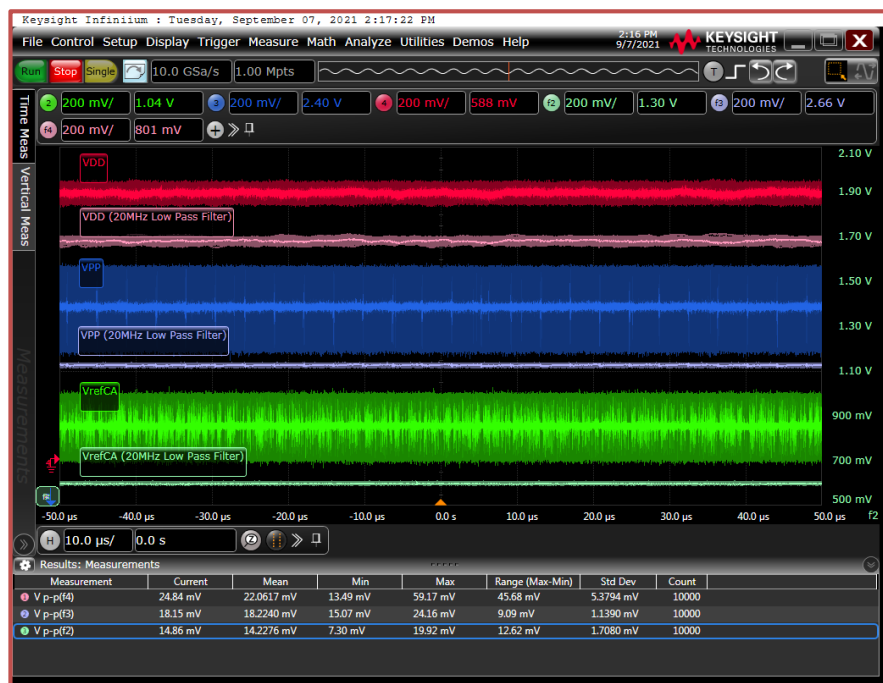
FAIL

- The clock period time of this system is 0.836ns and operating frequency is about 1196MHz. So, we applied with DDR4-2400 criteria value of JEDEC standard.
- This system doesn't have the power switch. So, we don't measure power-up sequence values.
- The VIX was NOT good and it did NOT meet the JEDEC standard. It must be improved. (Please refer to page#8)

Measurement Item	Result	Remark
Power Up Sequence Check	N/A	
Power Noise Check	Spec In.	- No problem.
Signal Integrity Check	Spec Out.	- The VIX was NOT good and it did NOT meet the JEDEC standard.

Power Noise Check Result

■ VDD / VPP / Vref_CA - with DRAM stress test

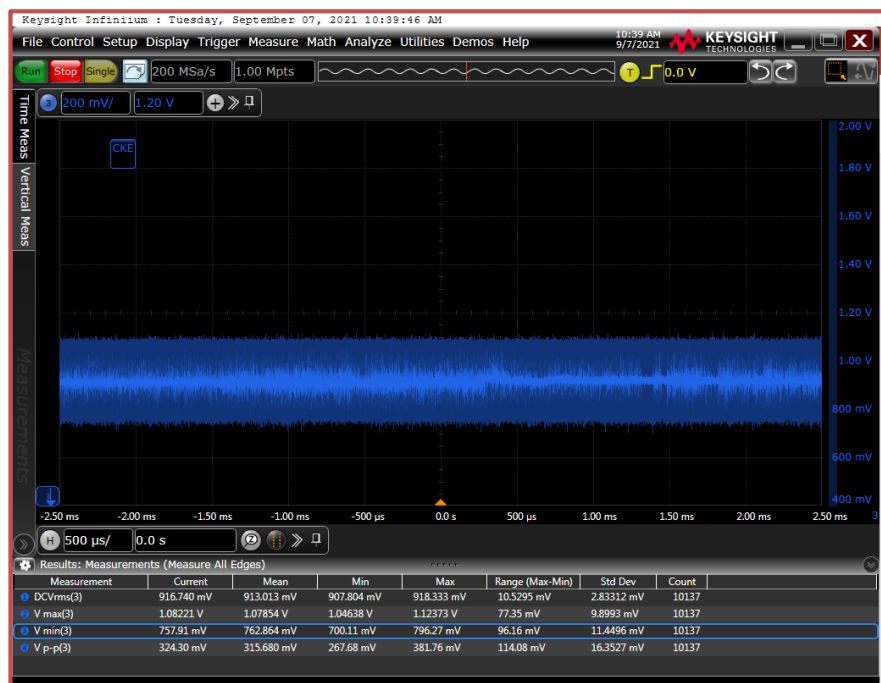


Parameter	Spec (AC+DC)	Peak to Peak	Remark
VDD	TBD	59mV	-
VPP	TBD	24mV	-
Vref-CA	≤ 24mV (VDD±1%)	20mV	Spec. in

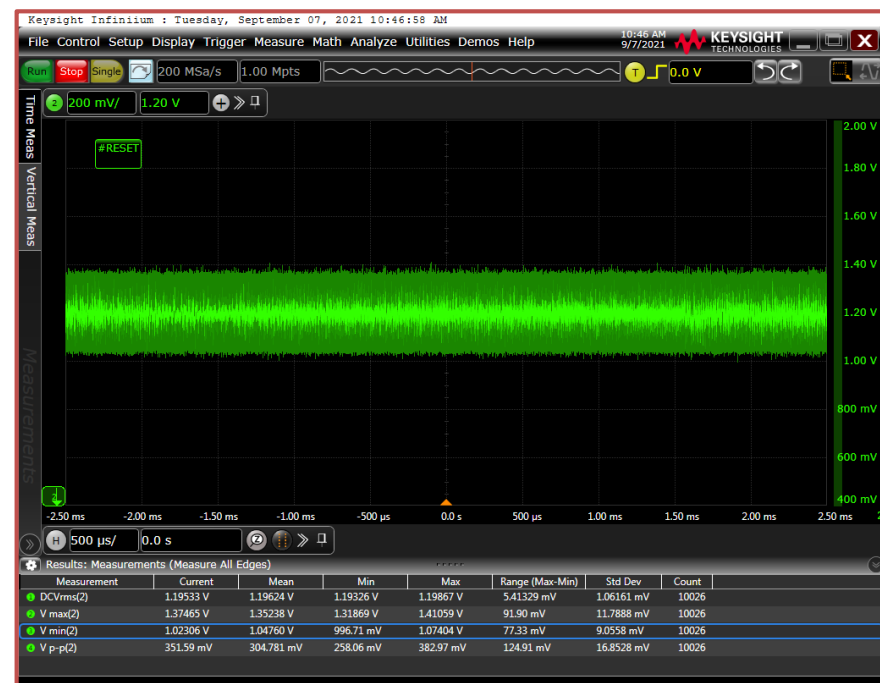
* SK hynix measured VDD/ VPP / Vref_CA including AC+DC (Low Pass Filter 20MHz) noise.

CKE & /RESET Signal Check Result

■ CKE Level in System Operation



■ /RESET Level in System Operation



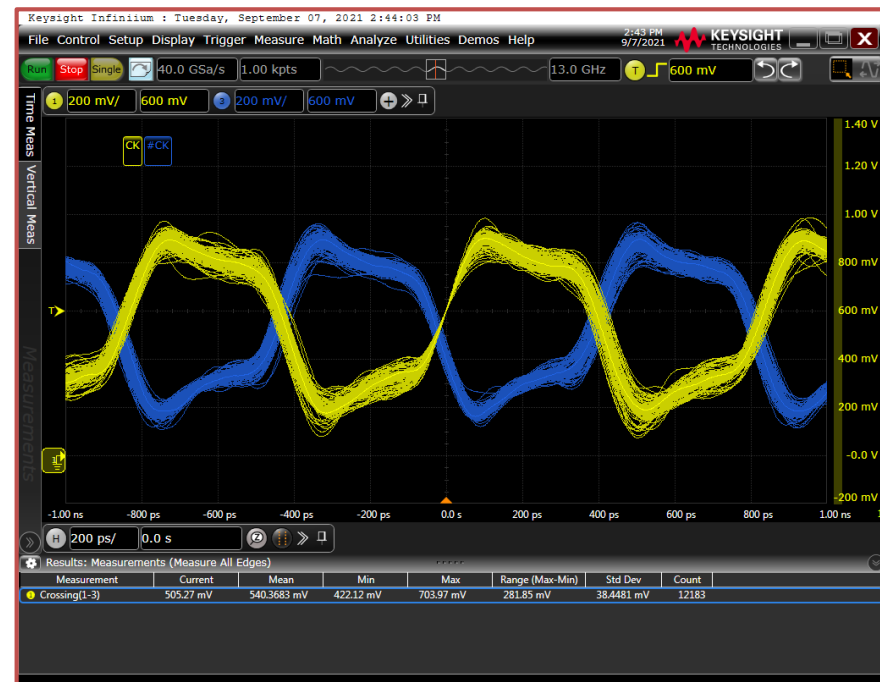
Parameter	Measurement	Remark
CKE Level	Vmin : 700mV	Power-down & Self-refresh mode not used.
/RESET Level	Vmin : 997mV	High state stable

Signal Integrity Test Result (Clock)

■ Clock with differential



■ Clock VIX



Parameter	Spec		Measurement	Remark
	Min	Max		
Clock Cycle Time (tCK)	0.833ns	0.937ns	0.836ns	Spec. in
Clock High Level Width (tCH)	401ps(0.48tCK)	435ps(0.52tCK)	421ps (0.503tCK)	Spec. in
Clock Low Level Width (tCL)	401ps(0.48tCK)	435ps(0.52tCK)	416ps (0.497tCK)	Spec. in
Clock Period Jitter (JIT_per)	-42ps	42ps	-37 / 40	Spec. in
VIH diff(ac)	0.200V	-	0.561V	Spec. in
VIL diff(ac)	-	-0.200V	-0.618V	Spec. in
Clock VIX	0.480V	0.720V	0.422V / 0.704V	Spec. out

Signal Integrity Test Result (Command / Address)

■ CS#_U2



■ RAS#_U2



Parameter	Spec.		Measurement		Remark
Unit : ps	Min	Max	CS#	RAS#	
tIS(Base)	62 ps	-	334ps	893ps	Spec. in
tIH(Base)	87 ps	-	321ps	326ps	Spec. in

Signal Integrity Test Result (Command / Address)

■ CAS#_U2



■ WE#_U2



Parameter	Spec.		Measurement		Remark
Unit : ps	Min	Max	CAS#	WE#	
tIS(Base)	62 ps	-	884ps	1263ps	Spec. in
tIH(Base)	87 ps	-	330ps	255ps	Spec. in

Signal Integrity Test Result (Command / Address)

■ ADD11_U2



Parameter	Spec.		Measurement	Remark
Unit : ps	Min	Max	ADD11	
tIS(Base)	62 ps	-	1175ps	Spec. in
tIH(Base)	87 ps	-	343ps	Spec. in

Signal Integrity Test Result (Data strobe / Data)

■ VIHL_AC_U2_DQL



■ VIHL_AC_U2_DQU



Parameter	Spec.		Measurement		Remark
Unit : mV	Min	Max	DQL	DQU	
VIHL	160 mV	-	712mV	748mV	Spec. in

Signal Integrity Test Result (Data strobe / Data)

■ TdIPW_U2_DQL



■ TdIPW_U2_DQU



Parameter	Spec.		Measurement		Remark
Unit : ps	Min	Max	DQL	DQU	
TdIPW	232 ps (0.58 UI)	-	334ps	338ps	Spec. in

Signal Integrity Test Result (Data strobe / Data)

■ TdIVW_total / VdIVW_total_U2_DQL ※ : Spec. Zone ■ TdIVW_total / VdIVW_total_U2_DQU



Parameter	Spec.		Measurement		Remark
Unit : ps, mV	Min	Max	DQL	DQU	
TdIVW_total	-	80 ps (0.2 UI)	Spec. In	Spec. In	1 UI = 400 ps
VdIVW_total	-	130 mV	Spec. In	Spec. In	Vcent_DQ = $\Delta V_{IHL}/2$

Signal Integrity Test Result (Data strobe / Data)

■ tDQSS_U2_DQSL



■ tDQSS_U2_DQSU



Parameter	Spec.		Measurement		Remark
Unit : ps	Min	Max	DQSL	DQSU	
tDQSS	-226 (-0.27tCK)	226 (+0.27tCK)	-101ps	-82ps	Spec. in

Thank you